Technical Performance Report

SUPERCONDUCTING/SEMICONDUCTING HYBRIDS AND ADVANCE MEMORY CONCEPTS FOR SUPERCONDUCTING ELECTRONICS

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INTRODUCTION

The goal of this program is to explore advanced alternatives to the standard approaches to memory in Josephson junction digital electronics. The work includes the physics, circuits and systems aspects of the problem.

It is widely recognized that memory is the weak suit of digital superconductive electronics. There are several problems. They are very hard to build, particularly at high densities. Their speed is being challenged by leading edge semiconductor memories, albeit at the expense of high power dissipation. They are susceptible to trapped flux, which is both random in space and likely varying in time. All the current approaches to memory are based on the concept of storage of magnetic flux in a superconducting ring first proposed over 25 years ago by Anacker. Basically, there have been no new ideas in superconductive memory since that time.

One obvious problem with the current JJ memory cells, based on storage of magnetic flux in a superconducting ring, is the large size of the cells required. The initial thrust of our program has been to address this particular problem. The large size results from the minimum inductance necessary to stably store a single flux quantum. We have proposed using the kinetic inductance of a superconductor as an alternative source of the required inductance. In this case the datum is stored in the kinetic energy of the superconducting electrons rather than in the magnetic energy. Since the kinetic inductance increases with decreasing linewidth, very compact cells are possible. The price paid for this approach is that magnetic coupling cannot be used to write or interrogate the cell. Direct current coupling must be used, at an attendant cost of loss of isolation. On the other hand, the kinetic inductance memory cell (KIMC) should be immune to the problems of flux trapping.

In the course of this work, we have also explored the potential of using ferromagnetic cores in the superconducting rings, so as to increase the inductance per unit length of a microstrip line and thereby decreasing the size of the cells. Others, such as the group at Berkeley, have been exploring the use of semiconductor memories and hybrid superconducting/semiconducting memory concepts operating at low temperatures as an alternative.

SUMMARY OF PROGRESS OVER THE PAST YEAR

Kinetic Inductance Memory Cell

During the past year, we have been working on the circuits needed to make a memory array from the KIMC. This circuit design was challenging because the basic memory cell requires current injection for both read and write access. Given a current injection architecture, the main problem that needed to be solved was isolation—how to access uniquely one cell in a large array. The solutions for reads and writes are different. For reads, one can interrogate multiple cells simultaneously but only look at the desired output using a multiplexer. For writes, the datum must be written to the correct cell.

The write isolation problem was ameliorated by using a non-linear resistor in series with the memory loop. The nonlinear resistor can be an SIS tunnel junction with its Josephson current suppressed, or two back-to-back SIN junctions. Using voltage drive on the array, the voltage across the selected cell is twice the half-selected case, and hence the ratio of selected to half-selected current can be large (10:1). This large current ratio allows one cell on a wordline to be written, while the other cells on the same wordline hold their old values.

The read port is built using two smaller junctions and some resistors that are placed in parallel with the main storage loop. These devices sense the current flowing in the main cell and are switched during a read operation if the cell is storing a one. Since there is no need to read a single cell on the wordline, the resistors in the original design were normal linear devices. We are reconsidering this decision, however, as described below.

Considerable work was done on the cell and the peripheral circuits to maximize the margins of the cell. This led to a design with good margins, at least +/- 20% on all parameters. Once this design was completed, we looked at the overall memory performance and were surprised. While the memory worked, the speed and power of the design were not very good. The problems were related to and were caused by the resistor-coupled current injection architecture that we used. Since each cell presented a resistive load to both the wordline and bitline, these lines act as distributed L/R lines and not as transmission lines. Hence the delay of a signal is proportional to the length of the line squared (since the inductance is proportional to length, and the effective shunt resistance is inversely proportional to length). These shunt resistors also mean that the wordline and bitline drivers need to supply the current that is required by all the shunt resistors, in addition to the current needed by the selected cell.

To drive the necessary large current, a high-power driver is required and since each driver uses current whether it is activated or not, the power dissipation of the memory is quite high. The fundamental origins of these problems is the lack of isolation. Use of a nonlinear resistor in the wordline readout circuit of each cell would reduce this problem considerably, reducing both the read access time and the total power required.

In addition to these circuit and memory architecture studies, we have designed and had fabricated 4×4 prototype kinetic inductance memory cell arrays. The circuits were fabricated by TRW at no cost to this contract. The storage inductors used will be magnetic, but since our current injection architecture was employed, the circuits will provide a substantive test our circuit read/write design. These chips have now been received and are ready for test.

Ferromagnetic Cores for Conventional Memory Cells

As an alternative approach to reducing the physical size of the inductors used in current superconductive magnetic memory cells, we have examined the feasibility of using ferromagnetic cores in the inductors. This approach is the analog of the use of ferroelectric dielectrics in the capacitors of semiconductor DRAM's to reduce their area. Also, since magnetic coupling is retained in this approach, the isolation problems detailed above do not arise.

It is obvious that one can reduce the size of an inductor by using a ferromagnetic core. The real question is whether there are ferromagnetic materials available that can provide a useful level of permeability at the high required switching speeds (below 1 nsec). The switching speed of ferromagnets is limited by the zero-field ferromagnetic resonance frequency, i.e., the Larmour frequency due to the intrinsic anisotropy of the material. Metallic ferromagnets have the further problem of eddy current decays. We have surveyed magnetic insulators. (These same materials are being examined by others for use as isolators and other passive elements in thin-film MIMC circuits.) For three-dimensional ferromagnets there is a theoretical limit to the ferromagnetic resonance frequency known as Snoek's law that says $f_r(\mu-1) = 10^9$ Hz. To get meaningful reductions in area, μ's of order 5 are sufficient, so that the speed is marginal. However, for two-dimensional magnets, precession of the spins does not occur and Snoek's limit formally becomes infinite.

After a literature search, we have identified a class of candidate two-dimensional ferromagnetic insulators. The magnets at issue (e.g., $Ba_3Co_2Fe_{24}O_{41}$) were discovered in the 1950's. Reported measurements of the complex permeability of these materials show that they have the desired speed. Preliminary attempts to laser ablate these materials have been undertaken, but the results have not yet been analyzed. Preliminary analyses of the total access time of conventional style superconducting memory cells using these ferromagnets indicate some potential for this approach in large, fast cache memories (e.g., 64 kB to 256 kB). We emphasize that the materials considered so far are not modern. A survey of the more contemporary two-dimensional magnet literature likely would lead to additional candidate materials. The issue of flux trapping has not yet been examined.

FUTURE WORK

In comparing our performance and power numbers with other memories that have been developed, we found that many of them were competitive with the KIMC in speed and power. This result is disappointing, since the high power dissipation in the small

memory would preclude building large superconducting memories. It is premature to declare that these problems are fundamental, however. We would like to explore using techniques that have been widely used in semiconductor memory design to alleviate similar problems in our superconducting memories. These techniques include partitioning, and partial array activation. By breaking the full memory array into a number of smaller subarrays, the word and bit lines can be made short enough that the wires act as transmission lines rather than L/R lines. Although the signals needed to activate each individual subarray may be long, these wires have a small number of loads and should also be able to operate in the transmission line domain.

The more difficult problem is power reduction, since it is hard to build Josephson logic that does not dissipate static power. (Josephson logic is relevant to memory because of its use in the decoder circuits.) We need to explore circuits that can route current to the desired array, rather than powering up all the arrays at once.

These problems with speed and power raise some interesting fundamental questions about superconducting logic. First, why does semiconductor memory seem to have a different set of limits on its performance than superconducting memory? A related question is, what are the fundamental limits in semiconductor technology? Clearly there must be some transmission line limits in this technology too, but they are never mentioned. We want to consider these issues.

Another interesting question is why superconducting memory is not a dual of its semiconductor cousin. It has long been known that formally such duality exists. We want to explore what happens when one tries to build the appropriate dual structures. For example, in CMOS circuits the gates are connected in parallel to the power supplies and route voltages to set signal levels. The gates take no current, except when they are switching, and thus the power is low. The dual of this environment is a system where gates are connected in series and there is a constant current flowing through them. The gates route current as a signal, and there is a voltage across the gate only when the gate is switching. If this type of connection strategy could be used in a memory circuit, there is a hope that both the speed and the power could be dramatically improved.

Finally, there is a new superconducting device that seems to offer qualitatively new opportunities. It is the so-called Superconducting Flux Flow Transistor (SFFT). Its operating characteristics are much more like a transistor, as its name implies. It is a true dual of a semiconducting FET. There are unpublished claims that these devices have been successfully fabricated in a 64 kB array with a reasonably successful bit yield using the high-Tc materials TBCCO. This is a remarkable claim. We propose to do a more thorough and systematic investigation of this approach to memory. We include considerations of the detailed physics of these devices, which will eventually set their fundamental limits, and to explore fabrication of such devices with low-Tc materials for use with LTS systems and as a model system for device physics studies. Niobium is known not to be a suitable material. We will examine NbN and the various alloys of Nb, which appear to be more favorable candidates—low flux flow viscosity and low pinning. For academic purposes, we could also look at amorphous Mo-Ge alloys, which we have been studying for other purposes for

many years. For technological purposes, NbN or alloys of Nb will be required in order to necessitate minimal changes in the LTS digital JJ materials technology.

Of course, SFFT's fit neatly into the new semiconductor design environment mentioned above, since the SFFT is the dual of an FET. It will be interesting to see how far this duality can be pushed in practical circuits.

COLLABORATIONS WITH THE BERKELEY GROUP

We have had a number of discussions with the Berkeley group, including exchange visits. On the basis of these discussions, we are now working out more formal connections and collaborative activities. In the fall we will begin monthly meetings to keep each other informed of progress. We also are exploring more explicit joint projects in superconductor/semiconductor hybrids and in exploration of the potential of SFFT's. We intend to combine aggressively the strong JJ circuit experience at Berkeley and the strong semiconductor memory and superconducting materials and device physics experience at Stanford.

PERSONNEL ISSUES

George Chen, whose thesis was involved in all aspects of the KIMC, has now received his PhD. George was advised jointly by Professors Beasley and Horowitz, and we feel such a arrangement can be generalized. George has taken a position at TRW but will stay on at Stanford as well as a 25%-time research associate. This arrangement couples the Stanford operation both with TRW and with the DoC ATP program on superconducting electronics between Conductus, TRW, NIST, Berkeley and Stanford. In our original proposal we imagined this role to be played by Dr. Steve Whiteley, but all agree this new arrangement is much better. There is no change in budget allocation required. Chen's salary will simply come from the original allocation for Whiteley as a consultant.

Wayne Felson, a Stanford Undergraduate with a double major in Physics and Computer Science and who did the analysis of the ferromagnetic cores in superconducting memory inductors, has now completed his degree and will enter graduate school at Cornell in the fall. He is currently spending the summer working at Hypres, Inc., in New York.

Bharadwaj Amrutur joined our program in the past year and will take the lead in exploring the utilization of advanced semiconductor memory concepts to superconducting memories.